SGS-THOMSON MICROELECTRONICS

QUALITY & RELIABILITY REPORT

July 1994 to June 1995 - EPROM, FLASH MEMORY, EEPROM and SRAM Products

INTRODUCTION

SGS-THOMSON manufactures a wide range of memory types which include:

Non-volatile memories: FLASH Memory, EPROM, OTP ROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; FLASH Memories in 1.2 to 0.6µ CMOS technology; OTP ROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Static RAMs: Fast SRAM, both Synchronous and Asynchronous and NVRAMs (ZEROPOWER and TIMEKEEPER ranges). Fast SRAMs are manufactured in 0.7-0.6µ HCMOS technology; NVRAMs in 1.2-0.8µ HCMOS.

Packages for Static RAM products include the plastic PDIP, PLCC and SOJ. Some of the ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from July 1994 to June 1995. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Table 1. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	215	0	174	0	16,916	0	8,370	0	9,278	0	4,452	0
		– 168 hrs	215	0	174	0	2,085	0	1,638	0	1,151	0	2,649	0
		– 500 hrs	215	0	174	0	1,136	0	351	0	1,151	0	585	0
		– 1000 hrs	215	0	174	0	1,019	0	351	0	1,151	0	468	0
Retention Bake	1008	250°C,												
		– 48 hrs	150	0	250	0	1,300	0	500	0	500	0	1,000	0
		– 168 hrs	150	0	250	0	1,300	0	500	0	500	0	1,000	0
		– 500 hrs	150	0	250	0	1,300	0	500	0	500	0	1,000	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 2. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	2,656	0
		– 168 hrs	500	0
		– 500 hrs	500	0
		– 1000 hrs	400	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	200	0
		– 168 hrs	200	0
		– 500 hrs	200	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 3. CMOS E5/0.8µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B (B) M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, (50% '0')		
		– 48 hrs	22,884	0
		– 168 hrs	400	0
		– 500 hrs	400	0
		– 1000 hrs	400	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C, (99% '0')		
		– 48 hrs	200	0
		– 168 hrs	200	0
		– 500 hrs	200	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 4. CMOS E5/0.8µm Process (-20% upgrade) UV EPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512 (C)		M27C1001 (C)		M27C1024 (B)		M27C2001 (C)		M27C4001 (D)		M27C4002 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	10,748	0	13,079	0	3,434	0	5,070	0	2,238	0	8,438	0
		– 168 hrs	1,200	0	2,222	1 (a)	200	0	296	0	768	0	122	0
		– 500 hrs	1,200	0	1,293	0	200	0	296	0	680	0	122	0
		– 1000 hrs	1,200	0	1,293	0	200	0	296	0	680	0	122	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	700	0	1,156	0	150	0	50	0	500	0	100	0
		– 168 hrs	700	0	1,156	0	150	0	50	0	500	0	100	0
		– 500 hrs	700	0	1,156	0	150	0	50	0	500	0	100	0
		– 1000 hrs	-	-	60	0	-	-	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Contact spiking (barrier defectivity)

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 5. CMOS E5/0.8µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)		M27C801		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	6,882	0	3,855	0	8,640	0	8,110	0	283	0
		– 168 hrs	1,728	0	267	0	1,941	0	266	0	283	0
		– 500 hrs	192	0	267	0	480	0	266	0	283	0
		– 1000 hrs	192	0	267	0	384	0	266	0	283	0
		– 2000 hrs	96	0	144	0	96	0	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	700	0	200	0	1,000	0	150	0	100	0
		– 168 hrs	700	0	200	0	1,000	0	150	0	100	0
		– 500 hrs	700	0	200	0	900	0	150	0	100	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 6. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,410 3,410 1,700	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Thermal Shock	1011	–55 to 125°C, – 60 cycles	 200	 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Salt Atmosphere	1009	Test Condition A, 35°C	25	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	700	0
Resistance to Solvents	2015	4 Solvent Solutions	220	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	100	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Environmental Sequence:				
1. Thermal Shock	1011	–55 to 125°C, 15 cycles		
2. Temperature Cycling	1010	–65 to 150°C, 100 cycles	50	0
3. Moisture Resistance	1004	–10 to 65°C, RH = 90%, 10 cycles of 24hrs		
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Mechanical Sequence:				
1. Mechanical Shock	2002	Test Condition B		
2. Vibration Variable Frequency	2007	Test Condition A	100	0
3. Constant Acceleration	2001	Test Condition E		
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Temperature Cycling	1010	–65 to 150°C, 10 cycles		
Constant Acceleration	2001	Test Condition E	105	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 7. CMOS E5/0.8µm Process (–10% Upgrade) OTP ROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	912	0
		– 500 hrs	912	0
		– 1000 hrs	864	0
		– 2000 hrs	240	0
Retention Bake	1008	150°C,		
		– 168 hrs	1,057	0
		– 500 hrs	1,057	0
		– 1000 hrs	1,057	0
		– 2000 hrs	217	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 8. CMOS E5/0.8µm Process (–10% Upgrade) OTP ROM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	748	0
		– 500 hrs	748	0
		– 1000 hrs	748	0
		– 2000 hrs	248	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	643	0
		– 96 hrs	643	0
		– 168 hrs	615	0
		– 240 hrs	167	0
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	1,560	0
		– 96 hrs	1,560	0
		– 168 hrs	1,560	0
		– 240 hrs	1,560	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	1,560	0
		– 500 cycles	1,560	0
		– 1000 cycles	1,200	0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	110	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	44	0
Resistance to Solvents	2015	4 Solvent Solutions	120	0

Table 9. CMOS E5/0.8µm Process (–20% Upgrade) OTP ROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz												
		– 168 hrs	384	0	428	0	384	0	138	0	384	0	576	0
		– 500 hrs	384	0	428	0	384	0	138	0	384	0	576	0
		– 1000 hrs	336	0	380	0	288	0	138	0	384	0	528	0
		– 2000 hrs	96	0	92	0	48	0	-	-	96	0	96	0
Retention Bake	1008	150°C,												
		– 168 hrs	600	0	540	0	470	0	150	0	420	0	710	0
		– 500 hrs	600	0	540	0	470	0	150	0	420	0	710	0
		– 1000 hrs	600	0	480	0	410	0	150	0	420	0	710	0
		– 2000 hrs	120	0	60	0	180	0	-	-	120	0	230	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 10. CMOS E5/0.8µm Process (–20% Upgrade) OTP ROM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	500	0	399	0	450	0	48	0	450	0	500	0
		– 500 hrs	500	0	399	0	450	0	48	0	450	0	500	0
		– 1000 hrs	500	0	390	0	450	0	48	0	450	0	500	0
		– 2000 hrs	150	0	100	0	100	0	-	-	50	0	100	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,												
		– 48 hrs	224	0	168	0	280	0	48	0	195	0	280	0
		– 96 hrs	224	0	168	0	280	0	48	0	195	0	280	0
		– 168 hrs	224	0	168	0	252	0	48	0	195	0	252	0
		– 240 hrs	140	0	28	0	84	0	48	0	55	0	56	0
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	800	0	420	0	531	0	75	0	475	0	600	0
		– 96 hrs	800	0	420	0	531	0	75	0	475	0	600	0
		– 168 hrs	800	0	420	0	531	0	75	0	475	0	600	0
		– 240 hrs	800	0	420	0	531	0	75	0	475	0	600	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	660	0	540	0	480	0	50	0	360	0	540	0
		– 500 cycles	660	0	540	0	480	0	50	0	360	0	540	0
		– 1000 cycles	600	0	540	0	420	0	50	0	360	0	480	0
Solderability:														
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 435/0											
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 115/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 300/0											

Table 11. CMOS E5/0.8µm Process (–35% Upgrade) OTP ROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz						
		– 168 hrs	207	0	295	0	144	0
		– 500 hrs	207	0	295	0	144	0
		– 1000 hrs	207	0	295	0	96	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	188	0	210	0	180	0
		– 500 hrs	188	0	210	0	180	0
		– 1000 hrs	188	0	210	0	180	0
		– 2000 hrs	-	-	-	-	-	-

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 12. CMOS E5/0.8µm Process (–35% Upgrade) OTP ROM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	147	0	172	0	150	0
		– 500 hrs	147	0	172	0	150	0
		– 1000 hrs	147	0	172	0	150	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	28	0	-	-	112	0
		– 96 hrs	28	0	-	-	112	0
		– 168 hrs	-	-	-	-	112	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	145	0	195	0	240	0
		– 96 hrs	145	0	195	0	240	0
		– 168 hrs	145	0	195	0	240	0
		– 240 hrs	-	-	-	-	240	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	145	0	190	0	180	0
		– 500 cycles	145	0	190	0	180	0
		– 1000 cycles	145	0	190	0	180	0
Solderability:								
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 245/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 125/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 96/0					

Table 13. CMOS T4/1.2µm Process FLASH MEMORY Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	58,905	0	108,066	0
		– 168 hrs	720	0	798	0
		– 500 hrs	720	0	798	0
		– 1000 hrs	720	0	798	0
		– 2000 hrs	144	0	192	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	747	0	1.441	0
		– 500 hrs	747	0	1,441	0
		– 1000 hrs	747	0	1,441	0
		– 2000 hrs	150	0	400	0
Write/Erase Cycling		1,000 cycles	5,236	0	18,623	2 (a)
		10,000 cycles	-	-	614	1 (b)
Retention Bake	1008	150°C, 36 hrs	5,236	0	18,623	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
a. Programming Failure, single bit failures.
b. Erasing Failure, single bit failures.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 14. CMOS T4/1.2µm Process FLASH MEMORY Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	746	0	560	0
		– 500 hrs	746	0	560	0
		– 1000 hrs	746	0	560	0
		– 2000 hrs	150	0	199	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	331	0	246	0
		– 96 hrs	331	0	246	0
		– 168 hrs	331	0	246	0
		– 240 hrs	165	0	110	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	560	0	360	0
		– 96 hrs	560	0	360	0
		– 168 hrs	560	0	360	0
		– 240 hrs	520	0	360	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	450	0	380	0
		– 500 cycles	450	0	380	0
		– 1000 cycles	450	0	380	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	-	-	-	-
		– 500 cycles	-	-	-	-
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 435/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 75/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 328/0			

Table 15. CMOS T5/0.8µm Process FLASH MEMORY Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	144,729	0	47,338	0
		– 168 hrs	1,325	0	96	0
		– 500 hrs	1,325	0	96	0
		– 1000 hrs	1,225	0	96	0
		– 2000 hrs	231	0	48	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	1,546	0	100	0
		– 500 hrs	1,546	0	100	0
		– 1000 hrs	1,546	0	100	0
		– 2000 hrs	444	0	50	0
Retention Bake	1008	250°C,				
		– 168 hrs	631	0	-	-
		– 500 hrs	631	0	-	-
		– 1000 hrs	448	0	-	-
		– 2000 hrs	263	0	-	-
Write/Erase Cycling		1,000 cycles	24,421	4 (a)	6,704	0
		10,000 cycles	939	4 (b)	81	0
Retention Bake	1008	150°C, 36 hrs	24,421	0	6,704	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
a. Programming Failure, single bit failure.
b. Erasing Failure, single bit failure.

Table 16. CMOS T5/0.8µm Process FLASH MEMORY Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	700	0	50	0
		– 500 hrs	700	0	50	0
		– 1000 hrs	700	0	50	0
		– 2000 hrs	100	0	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	335	0	55	0
		– 96 hrs	335	0	55	0
		– 168 hrs	335	0	55	0
		– 240 hrs	168	0	55	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	1,134	0	80	0
		– 96 hrs	1,134	0	80	0
		– 168 hrs	1,134	0	80	0
		– 240 hrs	1,103	0	80	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	990	0	60	0
		– 500 cycles	990	0	60	0
		– 1000 cycles	690	0	60	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	-	-	-	-
		– 500 cycles	-	-	-	-
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 524/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 291/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 324/0			

Table 17. CMOS F3/1.5µm Process EEPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06 ST93C46A ST93CS46A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, – 24 hrs – 168 hrs – 500 hrs	 2,150 150 150	 0 0 0
Retention Bake	1008	150°C, – 500 hrs – 1000 hrs	 100 100	 0 0
Write/Erase Cycling		1,000,000 cycles	100	0
Retention Bake	1008	150°C, 168 hrs	100	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 18. CMOS F3/1.5µm Process EEPROM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06 ST93C46A ST93CS46A	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
Pressure Pot		121°C, 2Atm, – 168 hrs – 240 hrs	 50 50	 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles	 50	 0
Solderability:				
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	-	-
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	50	0
Resistance to Solvents	2015	4 Solvent Solutions	48	0
Resistance to Surface Mount				
– SO Package			125	0

Table 19A. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	100	0	8,700	0	2,400	0	-	-
		– 168 hrs	100	0	1,700	0	400	0	-	-
		– 500 hrs	100	0	1,700	0	400	0	-	-
		– 1000 hrs	-	-	228	0	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	-	-	1,680	0	400	0	100	0
		– 500 hrs	-	-	1,680	0	400	0	100	0
		– 1000 hrs	-	-	1,680	0	400	0	100	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	1,350	0	400	0	50	0
		1,000,000 cycles	-	-	1,350	0	400	0	50	0
Retention Bake	1008	150°C, 168 hrs	-	-	1,350	0	400	0	50	0

Table 19B. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28C64C		ST93C06C ST93C46C		ST95P04C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	-	-	8,800	0	74	0
		– 168 hrs	-	-	2,800	0	74	0
		– 500 hrs	-	-	2,800	0	74	0
		– 1000 hrs	-	-	-	-	74	0
Retention Bake	1008	150°C,						
		– 168 hrs	727	0	1,000	0	120	0
		– 500 hrs	727	0	1,000	0	120	0
		– 1000 hrs	727	0	1,000	0	120	0
		– 2000 hrs	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	700	0	1,150	0	49	0
		1,000,000 cycles	-	-	1,150	0	49	0
Retention Bake	1008	150°C, 168 hrs	700	0	1,150	0	49	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164		M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	-	-	1,215	0	120	0	135	0	442	0	1,490	0
		– 500 hrs	-	-	1,215	0	120	0	135	0	442	0	1,490	0
		– 1000 hrs	-	-	1,215	0	120	0	135	0	442	0	1,490	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	50	0	1,879	0	350	0	550	0	1,587	0	950	0
		– 96 hrs	50	0	1,879	0	350	0	550	0	1,587	0	950	0
		– 168 hrs	50	0	1,879	0	350	0	550	0	1,587	0	950	0
		– 240 hrs	50	0	1,879	0	350	0	550	0	1,587	0	950	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	50	0	2,200	0	350	0	550	0	1,500	0	900	0
		– 200 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,												
		– 500 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Solderability:														
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 588/0											
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 416/0											
– PLCC Package			Cumulative Sample/Fail = 75/0											
– TSOP Package			Cumulative Sample/Fail = 166/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 168/0											
Resististance to Surface Mount:														
– SO Package			Cumulative Sample/Fail = 975/0											
– TSOP Package			Cumulative Sample/Fail = 123/0											

Table 21. CMOS F45/1.0µm Process EEPROM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01F ST24W01F		ST24C02F ST24W02F		ST24C04F ST24W04F		ST24C08F		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 24 hrs	-	-	50	0	49	0	224	0	72	0
		– 168 hrs	-	-	50	0	49	0	224	0	72	0
		– 500 hrs	-	-	50	0	49	0	224	0	72	0
		– 1000 hrs	-	-	-	-	49	0	224	0	-	-
Retention Bake	1008	150°C,										
		– 168 hrs	-	-	-	-	-	-	-	-	60	0
		– 500 hrs	-	-	-	-	-	-	-	-	60	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	50	0	100	0	-	-	-	-	58	0
		1,000,000 cycles	-	-	100	0	-	-	-	-	58	0
Retention Bake	1008	150°C, 168 hrs	50	0	100	0	-	-	-	-	58	0

Table 22. CMOS F45/1.0µm Process EEPROM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C02F ST24W02F		ST24C04F ST24W04F		ST24E32F	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	-	-	-	-	80	0
		– 500 hrs	-	-	-	-	80	0
		– 1000 hrs	-	-	-	-	80	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	100	0	50	0	300	0
		– 96 hrs	100	0	50	0	300	0
		– 168 hrs	100	0	50	0	300	0
		– 240 hrs	100	0	50	0	300	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	100	0	-	-	200	0
		– 200 cycles	-	-	-	-	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability:								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = -/-					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 96/0					
– PLCC Package			Cumulative Sample/Fail = -/-					
– TSOP Package			Cumulative Sample/Fail = -/-					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-					
Resististance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 100/0					
– TSOP Package			Cumulative Sample/Fail = -/-					

Table 23. CMOS SPECTRUM/2.0μm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48Z02		MK48T02	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz				
		– 168 hrs	154	0	154	0
		– 500 hrs	154	0	153	0
		– 1000 hrs	154	0	153	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 24. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48Z02		MK48T02	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 154 154 154	 0 0 0	 154 154 154	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 154 154	 0 0	 154 153	 1 (a) 1 (b)
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 96/0			

Notes: a. B-pkg battery failure. Changing product to caphat will eliminate welding failures.
b. B-pkg solder joint failure. Solder joint had improper amount of solder for joint formation.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 25. HCMOS S3/1.2µm Process ZEROPOWER SRAM and FIFO Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08		MK48Z08		MK45H01	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1KHz						
		– 168 hrs	154	0	154	0	77	0
		– 500 hrs	154	0	154	0	77	0
		– 1000 hrs	154	0	154	0	77	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 26. HCMOS S3/1.2µm Process ZEROPOWER SRAM and FIFO Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08		MK48Z08		MK45H01	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 100 100 100	 0 0 0	 154 154 154	 0 0 0	 77 77 77	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 100 100	 0 0	 134 134	 0 0	 77 77	 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs	 - -	 - -	 - -	 - -	 89 89	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 140/0					

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 27. HCMOS 4P/0.7µm Process SRAM Reliability Data, Die Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256		MK62486	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz				
		– 168 hrs	497	1 (a)	154	0
		– 500 hrs	419	1 (b)	154	0
		– 1000 hrs	265	2 (c)	154	0

Notes: a. Single bit, suspected particle related failure.
b. Pattern fail to be confirmed.
c. Single bit and speed fail, suspected particle related failures.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 28. HCMOS 4P/0.7µm Process SRAM Reliability Data, Package Related Tests, July 1994 to June 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256		MK62486	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 154 154 154	 0 0 0	 77 77 77	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 - -	 - -	 89 -	 0 -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 334 273	 0 0	 154 154	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 48/0			

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

STATISTICAL PROCESS CONTROL

NMOS E3/1.5µm Process UV EPROM, Rousset - France Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Gate Oxide Thickness	1.38	1.32	1.34	1.29	1.25	1.04	2.38	2.22
Interpoly Oxide Thickness	1.21	1.11	2.05	1.11	1.53	1.45	2.06	1.80
Field Oxide Thickness	2.03	1.94	1.78	1.59	1.68	1.52	2.48	2.46
Intermediate Dielectric Thickness	3.64	3.57	4.52	4.40	7.28	7.02	5.31	5.11
Final P-Vapox Thickness	1.67	1.61	6.06	4.90	3.99	3.76	4.30	4.23
Polysilicon I Thickness	1.41	1.37	2.82	2.77	1.43	1.39	1.97	1.71
Polysilicon II Thickness	2.07	2.01	2.47	2.36	1.89	1.82	2.30	2.12
Aluminium 1% Si Thickness (SP1)	2.21	2.11	2.31	2.18	2.09	1.97	2.95	2.74
Polysilicon II Critical Dimensions	2.21	1.86	1.88	1.55	2.20	1.80	2.21	1.91
Active Area Critical Dimensions	1.65	1.61	3.67	3.13	1.44	1.36	3.18	3.13

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT Henancement 25 x 25 µm	2.92	2.85	2.17	2.13	2.98	2.78	2.46	2.46
VT Array 25 x 25 µm	4.03	3.81	2.85	2.45	4.50	4.06	4.25	3.75
VT Field	6.10	2.86	7.83	3.77	11.80	5.12	5.13	2.52
I_{DON} Depletion 25 x 25 µm (1)	0.97	0.96	2.35	2.12	2.94	2.71	3.13	2.77
Polysilicon II Sheet Resistance	11.60	3.22	13.30	3.58	13.30	3.47	13.50	3.55
Buried Contact Chain Resistance	28.70	5.51	25.10	4.88	36.60	6.85	34.50	6.49
N+ Sheet Resistance	9.68	8.08	7.77	6.39	3.07	2.59	8.98	7.23
AL-Polysilicon II Contact Chain Resistance	9.31	4.02	9.91	4.55	12.80	5.74	10.80	5.07
AL-N+ Contact Chain Resistance	8.45	6.52	6.52	5.29	7.64	6.26	7.76	6.33

Note: 1. Probe card problem at electrical test before EWS.

Big oscillation quarter to quarter of CP/CPK on resistances are due to test problems and the difficulty to screen these wrong values.

STATISTICAL PROCESS CONTROL

CMOS E5/0.8µm Process UV EPROM and OTP ROM, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.20	2.27	2.26	2.20	2.23	2.22	3.17	3.10
Silicon Nitride Thickness	1.54	1.52	2.00	1.96	2.01	1.99	2.03	2.02
Field Oxide Thickness	1.51	1.41	1.37	1.34	1.41	1.40	1.85	1.81
Gate Oxide Thickness	2.32	2.31	2.02	1.89	2.01	1.95	2.34	2.24
Interpoly Oxide Thickness	1.60	1.59	1.59	1.57	1.90	1.82	1.67	1.56
Intermediate Dielectric Thickness	2.48	2.35	1.79	1.76	2.08	2.02	2.08	1.99
Polysilicon I Thickness	1.41	1.36	1.65	1.60	1.72	1.64	2.17	2.14
Active Area Critical Dimensions	2.75	2.32	1.97	1.74	1.94	1.69	3.24	3.15
Policide Critical Dimensions	2.45	2.26	1.80	1.62	1.53	1.41	2.46	2.27

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	3.23	2.71	4.66	4.03	2.55	2.19	2.53	2.38
VT P-Channel 25 x 25 µm	2.27	2.00	2.04	1.86	2.58	2.14	2.00	1.54
VT Natural 25 x 25 µm	4.57	4.16	3.92	3.54	4.25	3.91	4.37	4.21
VT Memory Cell 0.8 x 0.8 µm	1.91	1.86	1.97	1.63	1.66	1.64	1.72	1.70
I_{DON} N-Channel 25 x 0.8 µm	3.40	2.84	3.23	3.05	3.10	2.98	3.12	2.90
N+ Active Area Contact Chain	4.42	3.36	3.82	3.35	5.73	4.46	7.07	5.39
AL-Tungsten Silicide Contact Chain Resistance	4.36	2.85	2.87	2.49	2.04	1.77	3.01	2.47

STATISTICAL PROCESS CONTROL

CMOS E5/0.8µm Process UV EPROM and OTP ROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.77	1.76	1.73	1.70	1.65	1.56	1.78	1.68
Silicon Nitride Thickness	1.96	1.94	1.57	1.40	1.50	1.34	1.47	1.41
Field Oxide Thickness	2.02	1.96	2.03	2.00	1.65	1.65	2.53	2.22
Gate Oxide Thickness	1.68	1.64	1.48	1.48	1.35	1.29	1.44	1.43
Interpoly Oxide Thickness	1.42	1.34	1.38	1.36	1.61	1.51	1.37	1.34
Intermediate Dielectric Thickness	1.71	1.69	1.81	1.59	1.85	1.81	1.75	1.68
Polysilicon I Thickness	2.60	2.57	2.98	2.96	2.80	2.74	2.63	2.58
Active Area Critical Dimensions	1.85	1.83	2.29	2.28	2.10	2.00	1.59	1.37
Policide Critical Dimensions	1.33	1.32	1.63	1.45	1.70	1.70	1.72	1.67

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.21	2.21	2.09	1.60	2.06	1.52	2.96	2.41
VT P-Channel 25 x 25 µm	2.06	1.84	2.20	1.77	2.70	2.24	3.28	3.22
VT Natural 25 x 25 µm	3.10	2.07	3.14	2.69	2.15	1.99	2.75	2.67
VT Memory Cell 0.8 x 0.8 µm	1.25	1.23	1.27	1.21	1.32	1.15	1.32	1.30
I_{DON} N-Channel 25 x 0.8 µm	2.71	2.53	1.84	1.73	2.02	1.94	2.52	2.39
N+ Active Area Contact Chain	4.10	2.54	4.51	3.87	6.04	5.29	4.39	3.78
AL-W Silicide Contact Chain Resistance	1.43	1.21	4.26	2.40	1.37	1.32	1.56	1.47

STATISTICAL PROCESS CONTROL

CMOS T4/1.2µm Process FLASH MEMORY, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.51	1.50	1.37	1.35	1.41	1.40	1.85	1.81
Polysilicon I Thickness	1.41	1.36	1.65	1.60	1.72	1.64	2.17	2.14
Gate Oxide Thickness	2.30	2.25	2.10	2.10	2.12	2.06	2.06	1.99
Tunnel Oxide Thickness	1.47	1.44	1.42	1.39	1.43	1.41	1.84	1.83
ONO Bottom Oxide Thickness	1.32	1.29	1.74	1.40	1.58	1.57	1.40	1.36
ONO Nitride Thickness	1.24	1.20	1.34	1.30	1.26	1.25	1.47	1.44
ONO Top Oxide Thickness	2.10	2.10	2.21	2.19	1.96	1.93	2.25	2.23
Active Area Critical Dimensions	1.45	1.43	1.97	1.45	1.56	1.54	1.65	1.54
Polysilicon II Critical Dimensions	1.43	1.37	1.80	1.60	1.54	1.52	1.69	1.64

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	3.64	3.00	2.67	2.09	2.24	2.22	1.88	1.80
VT P-Channel 25 x 25 µm	1.74	1.72	1.74	1.43	1.92	1.85	1.72	1.68
BV N-Channel 25 x 1.2 µm	1.56	1.43	1.45	1.41	1.44	1.41	1.44	1.39
BV P-Channel 25 x 1.6 µm	6.78	4.51	4.34	3.95	3.97	3.95	5.97	5.71
VT Memory Cell 0.8 x 0.8 µm	1.78	1.41	1.39	1.37	1.20	1.18	1.50	1.38
I_{DON} N-Channel 25 x 1.2 µm	1.80	1.67	2.04	1.34	1.78	1.78	1.71	1.70
Al-N+ Contact Chain	1.47	1.25	1.51	1.36	1.35	1.34	1.36	1.34
AL-W Silicide Contact Chain Resistance	1.54	1.48	1.53	1.45	1.45	1.43	1.65	1.63

STATISTICAL PROCESS CONTROL

CMOS T5/0.8µm Process FLASH MEMORY, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.51	1.50	1.37	1.35	1.41	1.40	1.85	1.81
Polysilicon I Thickness	1.41	1.36	1.65	1.60	1.72	1.64	2.17	2.14
Gate Oxide Thickness	2.30	2.25	2.10	2.10	2.12	2.06	2.06	1.99
Tunnel Oxide Thickness	1.47	1.44	1.42	1.39	1.43	1.41	1.84	1.83
ONO Bottom Oxide Thickness	1.32	1.29	1.74	1.40	1.58	1.57	1.40	1.36
ONO Nitride Thickness	1.24	1.20	1.34	1.30	1.26	1.25	1.47	1.44
ONO Top Oxide Thickness	2.10	2.10	2.21	2.19	1.96	1.93	2.25	2.23
Active Area Critical Dimensions	1.46	1.38	1.83	1.40	1.44	1.42	1.65	1.59
Polysilicon II Critical Dimensions	2.09	1.92	1.62	1.39	1.18 (1)	0.87	1.35	1.29

Note: 1. Low CPK is due to change of dimensional target to improve the access time.

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.64	2.11	2.38	1.81	2.80	2.79	1.69	1.55
VT P-Channel 25 x 25 µm	2.38	2.13	2.27	2.01	1.89	1.77	1.15 (1)	1.04 (1)
BV N-Channel 25 x 0.8 µm	4.94	4.33	4.54	3.90	4.59	4.59	3.56	3.48
BV P-Channel 25 x 0.9 µm	3.01	2.44	2.86	2.61	5.70	5.64	2.96	2.87
VT Memory Cell 0.8 x 0.8 µm	2.80	2.23	1.88	1.71	2.10	2.04	1.91	1.83
I_{DON} N-Channel 25 x 1.2 µm	3.00	2.55	2.24	1.84	2.24	2.14	1.45	1.34
Al-N+ Contact Chain	4.49	4.18	4.59	4.15	2.89	2.80	3.78	3.64
Al-W Silicide Contact Chain Resistance	1.80	1.59	2.56	2.50	2.62	2.60	4.45	4.36

Note: 1. Some runs with high variability of this parameter on furnace 5. A specific analysis is running.

STATISTICAL PROCESS CONTROL

UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Shear Test (D.A.)	(*)	3.69	(*)	5.00	(*)	3.66	(*)	2.82
Bond Strength (W.B.)	(*)	2.63	(*)	2.77	(*)	2.59	(*)	2.51
SN Thickness (Tin Plate)	1.75	1.63	1.70	1.85	1.62	1.43	1.56	1.43
Lead Lenght (Cropping)	2.55	1.55	2.00	2.80	1.78	2.66	3.67	2.20

Note: *. One side limit only (CPL).

FAILURE RATE PREDICTIONS

July 1994 to June 1995

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -20%	5.79	140	0.6	4.0	1,590	1	1.3	2.4
CMOS E5 -35%	3.40	140	0.6	4.0	932	0	1.0	2.5
NMOS E3	5.73	140	0.6	2.6	741	0	1.3	3.1
OTP								
CMOS E5 -20%	2.60	140	0.6	4.0	674	0	1.3	3.4
CMOS E5 -35%	0.62	140	0.6	4.0	161	0	5.6	14.0
FLASH								
CMOS T4	5.82	140	0.6	3.0	1,132	0	0.8	2.0
CMOS T5	6.27	140	0.6	4.0	1,626	0	0.6	1.4
SRAM								
CMOS Spectrum	0.31	125	0.7	4.0	95	0	9.6	24.0
HCMOS S3	0.38	125	0.7	4.0	118	0	7.7	19.0
HCMOS S4P	0.51	125	0.7	5.7	224	4	23.0	35.0
EEPROM								
CMOS F4	3.20	140	0.6	3.0	753	0	1.2	3.0